AMENDMENTS TO THE CLAIMS

Claims 1-15 (Cancelled)

16. (Currently Amended) An anti-fuse ~~formed on a first semiconductor material of a first conductivity type, the anti-fuse~~ comprising:

a ~~well formed in the~~ first semiconductor material~~, the well~~ having a surface, a ~~second~~ first conductivity type, and a dopant concentration;

a first doped region of the ~~second~~ first conductivity type formed in the ~~well~~ first semiconductor material, the first doped region having a dopant concentration that is greater than the dopant concentration of the ~~well~~ first semiconductor material;

a second doped region of ~~the first~~ a second conductivity type formed in the ~~well~~ first semiconductor material, the second doped region being spaced apart from the first doped region;

a third ~~doped~~ region formed in the ~~well~~ first semiconductor material, the third ~~doped~~ region being spaced apart from the first and second doped regions;

~~a layer of~~ an insulation material ~~formed on~~ that contacts the surface of the ~~well~~ first semiconductor material, the ~~layer of~~ insulation material having a first opening that exposes the first doped region ~~of the well~~, a second opening that exposes the second doped region ~~of the well~~, and a third opening that exposes the third ~~doped~~ region ~~of the well~~;

a first section of a second semiconductor material ~~formed on the layer of~~ that contacts the insulation material and the first doped region;

a second section of the second semiconductor material ~~formed on the layer of~~ that contacts the insulation material and the second doped region, the second section being spaced apart from the first section; and

~~a first layer of dielectric~~ an isolation material ~~formed on~~ that contacts the first section, the second section, and the third ~~doped~~ region.

17. (Currently Amended) The anti-fuse of claim 16 wherein the first section includes:

a first polysilicon region; and

a first ~~layer of silicide formed on~~ silicide region that contacts the first polysilicon region.

18. (Currently Amended) The anti-fuse of claim 17 wherein the second section includes:

a second polysilicon region; and

a second ~~layer of silicide formed on~~ silicide region that contacts the second polysilicon region.

19. (Currently Amended) The anti-fuse of claim 18 ~~and further comprising a third layer of silicide formed on~~ wherein the third ~~doped~~ region has a dopant concentration greater than the dopant concentration of the first semiconductor material and a third silicide region.

20. (Original) The anti-fuse of claim 19 and further comprising a side wall spacer formed to adjoin the first section over the third doped region.

21. (Cancelled.)

22. (Currently Amended) An anti-fuse ~~formed on a semiconductor material of a first conductivity type, the anti-fuse~~ comprising:

a ~~well formed in the~~ semiconductor material~~, the well~~ having a surface, a ~~second~~ first conductivity type, and a dopant concentration;

a first doped region of the ~~second~~ first conductivity type formed in the ~~well~~ semiconductor material, the first doped region having a dopant concentration that is greater than the dopant concentration of the ~~well~~ semiconductor material; ~~and~~

a second doped region of ~~the first~~ a second conductivity type formed in the ~~well~~ semiconductor material, the second doped region being spaced apart from the first doped region;

a third doped region formed in the ~~well~~ semiconductor material between the first and second doped regions, the third doped region having a top surface, no region having the first conductivity type and a dopant concentration greater than the semiconductor material lying between the second and third doped regions;

a metallic ~~layer formed on~~ material that contacts the third doped region; and

~~a layer of~~ an insulation material ~~formed on~~ having a bottom surface that contacts the metallic ~~layer~~ material, the ~~layer of~~ insulation material being free of a ~~conductive material that extends through the layer of insulation material and contacts the metallic layer~~ side wall surface that contacts the metallic material at a plurality of different vertical distances away from the top surface of the third doped region.

23. (Currently Amended) The anti-fuse of claim 22 wherein the third doped region has the ~~second~~ first conductivity type and a dopant concentration greater than the dopant concentration of the ~~well~~ semiconductor material.

24. (Cancelled).

25. (Currently Amended) The anti-fuse of claim 22 and further comprising:

a first region of conductive material ~~formed on~~ that contacts the first doped region, the first region of conductive material having sidewalls; and

a second region of conductive material ~~formed on~~ that contacts the second doped region, the second region of conductive material having sidewalls and being spaced apart from the first region of conductive material.

26. (Currently Amended) The anti-fuse of claim 25 and further comprising a first sidewall spacer ~~formed to contact~~ that contacts the sidewalls of the first region of conductive material.

27. (Currently Amended) The anti-fuse of claim 26 and further comprising a second sidewall spacer ~~formed to contact~~ that contacts the sidewalls of the second region of conductive material.

28. (Cancelled).

29. (Cancelled).

30. (Cancelled).

31. (Currently Amended) An anti-fuse ~~formed on a semiconductor material of a first conductivity type, the anti-fuse~~ comprising:

a ~~well formed in the~~ semiconductor material~~, the well~~ having a surface, a ~~second~~ first conductivity type, and a dopant concentration;

a first doped region of the ~~second~~ first conductivity type formed in the ~~well~~ semiconductor material, the first doped region having a dopant concentration that is greater than the dopant concentration of the ~~well~~ semiconductor material;

a second doped region of ~~the first~~ a second conductivity type formed in the ~~well~~ semiconductor material, the second doped region being spaced apart from the first doped region, no metallic region contacting the first and second doped regions;

a third doped region formed in the ~~well~~ semiconductor material, the third doped region being spaced apart from the first and second doped regions and having a dopant concentration that is greater than the dopant concentration of the ~~well~~ semiconductor material;

a metallic material ~~formed on~~ that contacts a metal region of the top surface of the third doped region, the metallic material having a top surface; and

~~a~~ an insulation region ~~of insulation material~~ that contacts the top surface of the metallic material, no conductive material contacting the top surface of the metallic material ~~over the metal region~~.

32. (Previously Added) The anti-fuse of claim 31 and further comprising:

a first conductive region that contacts the first doped region, the first conductive region being spaced apart from the third doped region and having a top surface; and

a second conductive region that contacts the second doped region, the second conductive region being spaced apart from the first conductive region and the third doped region and having a top surface.

33. (Currently Amended) The anti-fuse of claim 32 wherein the insulation region ~~of insulation material~~ lies between the first conductive region and the second conductive region.

34. (Previously Added) The anti-fuse of claim 33 and further comprising:

a first sidewall spacer that contacts a sidewall of the first conductive region; and

a second sidewall spacer that contacts a sidewall of the second conductive region.

35. (Previously Added) The anti-fuse of claim 34 wherein the metal region lies between the first and second sidewall spacers.

36. (Currently Amended) The anti-fuse of claim 32 and further comprising a first isolation region that lies between the first conductive region and the ~~well~~ semiconductor material.

37. (Currently Amended) The anti-fuse of claim 36 and further comprising a second isolation region that lies between the second conductive region and the ~~well~~ semiconductor material.

38. (Currently Amended) The anti-fuse of claim 32 and further comprising:

a first metallic region that contacts the top surface of the first conductive region; and

a second metallic region that contacts the top surface of the ~~first~~ second conductive region.

39. (Currently Amended) The anti-fuse of claim ~~38~~ 25 and further comprising a conductive metallic path that extends through the first ~~conductive~~ region of conductive material to contact the metallic material.

40. (Currently Amended) The anti-fuse of claim 39 and further comprising a conductive metallic path that extends through the second ~~conductive~~ region of conductive material to contact the metallic material.

41. (New) An anti-fuse comprising:

a semiconductor material having a top surface, a first conductivity type, and a dopant concentration;

a first doped region, the first doped region having the first conductivity type, being located in the semiconductor material, having a dopant concentration that is greater than the dopant concentration of the semiconductor material, and contacting the top surface of the semiconductor material;

a second doped region, the second doped region having a second conductivity type, being located in the semiconductor material, contacting the top surface of the semiconductor material, and being spaced apart from the first doped region;

a metallic structure that contacts the top surface of the semiconductor material between the first doped region and the second doped region, the metallic structure having a top surface; and

an insulation region that contacts all of the top surface of the metallic structure, the insulation region having a top surface.

42. (New) The anti-fuse of claim 41 and further comprising:

a first conductive region that contacts the first doped region, the first conductive region having a top surface; and

a second conductive region that contacts the second doped region, the second conductive region being spaced apart from the first conductive region and having a top surface,

the top surface of the metallic structure lying below the top surfaces of the first and second conductive regions, and the insulation region lying horizontally between the first and second conductive regions.

43. (New) The anti-fuse of claim 42 and further comprising:

a first metallic section that contacts the top surface of the first conductive region; and

a second metallic section that contacts the top surface of the second conductive region, all of the top surface of the metallic structure lying below the top surfaces of the first and second metallic sections.

44. (New) The anti-fuse of claim 43 wherein the insulation region contacts the first and second metallic sections and includes a plurality of openings that expose regions on the first and second metallic sections.

45. (New) The anti-fuse of claim 44 and further comprising a plurality of contacts located in the plurality of openings, the plurality of contacts having top surfaces, and bottom surfaces that contact the first and second metallic sections, the top surface of the metallic structure lying below the bottom surfaces of the contacts.

46. (New) The anti-fuse of claim 42 and further comprising:

a first sidewall spacer that contacts a sidewall of the first conductive region; and

a second sidewall spacer that contacts a sidewall of the second conductive region, the metallic structure lying between the first and second sidewall spacers, all of the top surface of the metallic structure lying below the top surfaces of the first and second conductive regions.

47. (New) The anti-fuse of claim 42 and further comprising:

a first sidewall spacer that contacts a sidewall of the first conductive region; and

a second sidewall spacer that contacts a sidewall of the second conductive region, the metallic structure lying between the first and second sidewall spacers, the insulation region contacting the first and second sidewall spacers and extending horizontally from a point on the first sidewall spacer to a point on the second sidewall spacer over all of the metallic structure.

48. (New) The anti-fuse of claim 47 and further comprising an isolation region that lies between the first conductive region and the semiconductor material.

49. (New) The anti-fuse of claim 43 and further comprising:

a first conductive metallic path that extends through the first conductive region after fusing, the first conductive metallic path contacting the first metallic section; and

a second conductive metallic path that extends through the second conductive region after fusing, the second conductive metallic path contacting the second metallic section.

50. (New) The anti-fuse of claim 41 wherein:

no metallic material contacts the first doped region prior to fusing;

no metallic material contacts the second doped region prior to fusing; and

no metallic material contacts the metallic structure prior to fusing.